Volume 10 Issue 3 (2022) 51-54 ISSN 2347 - 3258
International Journal of Advance Research and Innovation

Low-power design of digital VLSI circuits

Garima Gautam, Rishi Sikka
Department of Electronics and Communication, Sanskriti University, Mathura (UP), India.

Article Info
Article history:
Received 12 January 2022
Received in revised form
28 June 2022
Accepted 5 July 2022
Available online 15 September 2022

Keywords: Low-Power Design, Clock Distribution, Timing Monitoring, Nanometer Nodes, Dynamic Clock Adjustment, Multipliers.

Abstract: With the increase of self-powered and intelligent devices, everyday life the forecaste, using implementation of energy-autonomous devices. Even though techniques such as voltage scaling proved to effectively reduce the energy consumption of digital circuits, additional energy savings are still required for a longer battery life. In this thesis, Digital systems tools is described to reduce the energy consumption and a variety of circuits, techniques, in when operated
inside the inexact region either in the conservative and safe exact region.This paper proposes techniques like MT-CMOS, power gating, dual stack, Galeor and Lector to reduce the leakage power. A D-Flip Flop has been designed using these techniques and power dissipation is calculated and is compared with general CMOS logic of D Flip Flop. Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent.

1. Introduction

The word digital has made a dramatic impact on our society. The increasing prominence of portable system and the need to limit power consumption in very-high density ULSI chips have led to rapid and innovative developments in low-power design during the recent years More significant is a continuous trend towards digital solutions in all areas –from electronic instrumentation, control, data manipulation, signals processing, telecommunications to consumer electronics. Development of such solutions has been possible due to good digital system design and modeling techniques power losses through the methodology

1.1 MT-CMOS

Multi-threshold CMOS (MTCMOS) power gating is a design technique in which a power gating transistor is connected between the logic transistors and either ground, thus can creating a virtual supply rail or virtual ground rail. Gating transistor sizing, transition current, short circuit current and transition time are design issues for power gating design. as sleep transistors to reduce the leakage power from the circuit and hence consuming very less power from the source. This technique acts as a very efficient method for reducing the consumption of power. The use of power gating design results in the delay overhead in the active mode. If both nMOS and PMOS sleeptransisto are used in power gating, delay overhead will increase. This paper proposes the design methodology for reducing the delay of the logic circuits during active mode. This methodology limits the maximum value of transition current to a specified value and eliminates short circuit current. Experiment results show 16.83% reduction in the delay.

1.2 Power Gating

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing. Operation to be seamlessly transformed into a fully DET clock gating has been fully integrated into the digital standard design flow for the first time. This is the design flow that has been proposed.

1.3 Dual-edge-triggered

Dual-edge-triggered clocking is a well-known method for reducing synchronous IC dynamic power dissipation. In contrast to the traditional single-edge-triggered. In contrast to the system, which samples data on DET operation samples data on both rising and falling edges of clock, requiring half the time of the system. Dual edge triggered is frequently secondary role is used only in synchronous design, specialized uses and products.

Corresponding Author,
E-mail address: gautamgarima32@gmail.com

DET clocking power quickly identify the characteristics of systems DET clocking to a conventional single-edge- triggered (SET) design in fully automated design. DET registers is proposed the flip-flop (DET-FF) that completely avoids clock-overlap .The aim of energy-quality scaling techniques small degra- dation on the QoS and lower energy consumption in digital circuits.

2.Proposed Dual-Edge Triggered Flip-Flop

These latches are designed using one transmission gate and two inverters connected back to back and the output of both the latches are connected 2:1Mux as input. Mux is designed using one PMOS and one NMOS connected in series and gates are connected together and derived by the inverted CLK. Output of Mux is connected to the inverter for strengthening the output.

Back to back connected inverters hold the data when transmission gate is OFF and at the same time Mux sends the latched data to the inverter to get the correct D at the output The proposed DETFF works as follows. When the CLK is low M3, M4 and M18 are ON and M5, M6 and M17 are OFF. Hence data hold by negative latch is transparent to Q. When CLK is high M5, M6 and M17 are ON and M3, M4 and M18 are OFF.

If input D remains the same, Q also remains unchanged. On the other hand, if D is changed before the CLK then D will be hold by positive latch and the same value will be send to the output when CLK changes from Low to high and similarly for the transition of CLK from high to low.

2.1 Automated Dual EdgeTriggered Clocking

Despite the fact that application are suitable Dual Edge Triggered Clocking, implementation of clock , as well as their integration into other systems. It is expected that the flow will be almost completely ignore. A minimum number of digital architectures that use DET clocking have been documented. These vast majority previous papers on DET clocking have concentrated in the design ignore the complexities of DET-based system integration with electronic design automation (EDA). Furthermore, most typical cell libraries only have SET storage elements and clock-gating circuits, making it difficult to define DET restrictions for clock-tree synthesis and static timing analysis ,particularly when clock- gate is used. Simulations are used. MC simulations are used to validate the storage cell's resilience against faults to demonstrate its durability. Second, In terms of performance and power consumption, the SDET- TSPCFF is compared. In comparison, all circuits built in a 40 nm CMOS process using standard-VT transistor. The comparison results with different DET-FFs show that the proposed SDET-TSPCFF not only solves the clock-overlap failures, but also has the lowest tcq. Because it relies heavily on tristate logic. As a result performance is limited at near-threshold operation. . The DET-latency ISLMs and power consumption are nearly identical to the DET-TGLMs, with the only difference being the output MUX

Because transmission gates have lower conductivity at scaled voltage supplies, the proposed circuit has a higher tcq than the DET-TGLM.

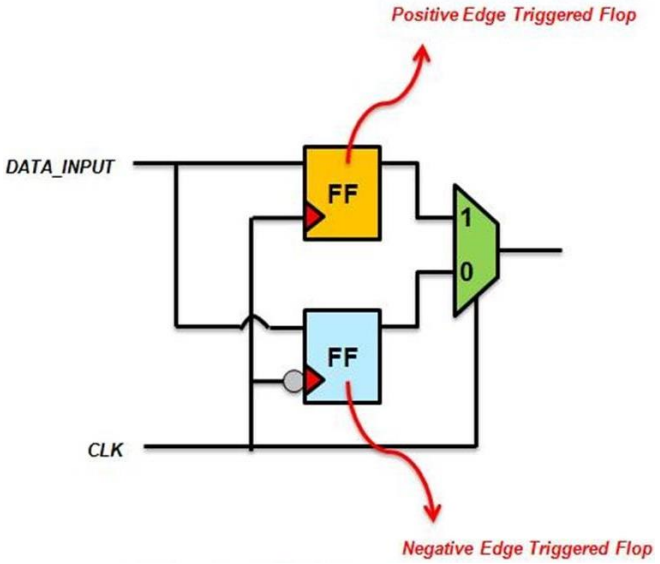

Fig.1: Dual edge trigerred Flip flop

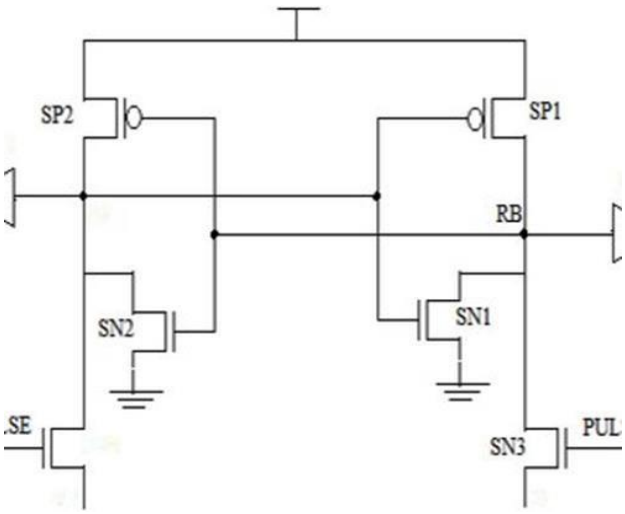

Fig.2: Low Power Dual-edge-triggered

A circle indicates that DET power consumptions are expected to be equal. In the CS-C registers power breakdown. When all blocks are included, power is save in the clock range then power save in the registers range, owing to the DET-FFs' lower operating requency and lower power consumption when compared to their SET counterparts, Time [ns].

SET implementation, due to the significant fraction of overall energy consumption of the clock tree and registers (A.7) significant total power reductions when implemented using DET clocking. The high number of registers and clock buffers result in large values of both E int and E dyn, as well as elevated activity factors. This is evident in mode of operation, where the DET design saves 56 percent on total power consumption, which drops to only 6 percent in the second operating mode, where clock-gating efficiency is significantly better. It's also worth noting that DET in CS-C saves a lot of power, using 58% less than the SET implementation. SET and The comparable SET frequency influences the DET/SET total power ratio. The operating points of the simulations are denoted by a cross, while the points where SET and 0.98.

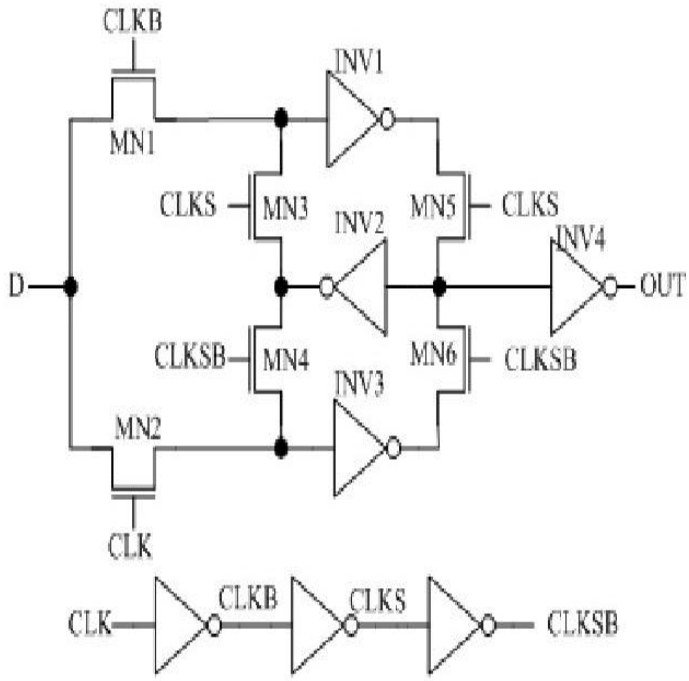

Fig. 3: Lower power Automation DET

Table 1: Number of SCs abd Register area with DET

Case Study	Number of SCs	Register Area	DET-SCs Area	Area Overhead
A	228 K	18.5 % 572,009 μm^2	642,505 μm^2	+ 12.3 %
B	24 K	17.3 % 48,764 μm^2	58,300 μm^2	+ 19.55%
C	37 K	9.4 %,52,245 μm^2	57,953 μm^2	+ 10.9 %

3.Design FIR LPF by windowing method and plot its magnitude and phase response-MATLAB Program

```
clc;
close all;
clear all;
fp= input ('Enter passband edge normalised freq. wp=');
n= input ('Enter order of filter=');
ps= input('Enter  sampling freq');
fn= 2*fp/ps;
window = blackman(n+1); %boxer, bartlett,
hanning,hamming,(use at place of blackman)
b = fir1(n,fn,window);
[h,w] = freqz(b,1,128);
Subplot(2,1,1);
plot(w/pi,angle(h));
Xlabel('Normalised freq…');
Ylabel('angle…');
```

Output

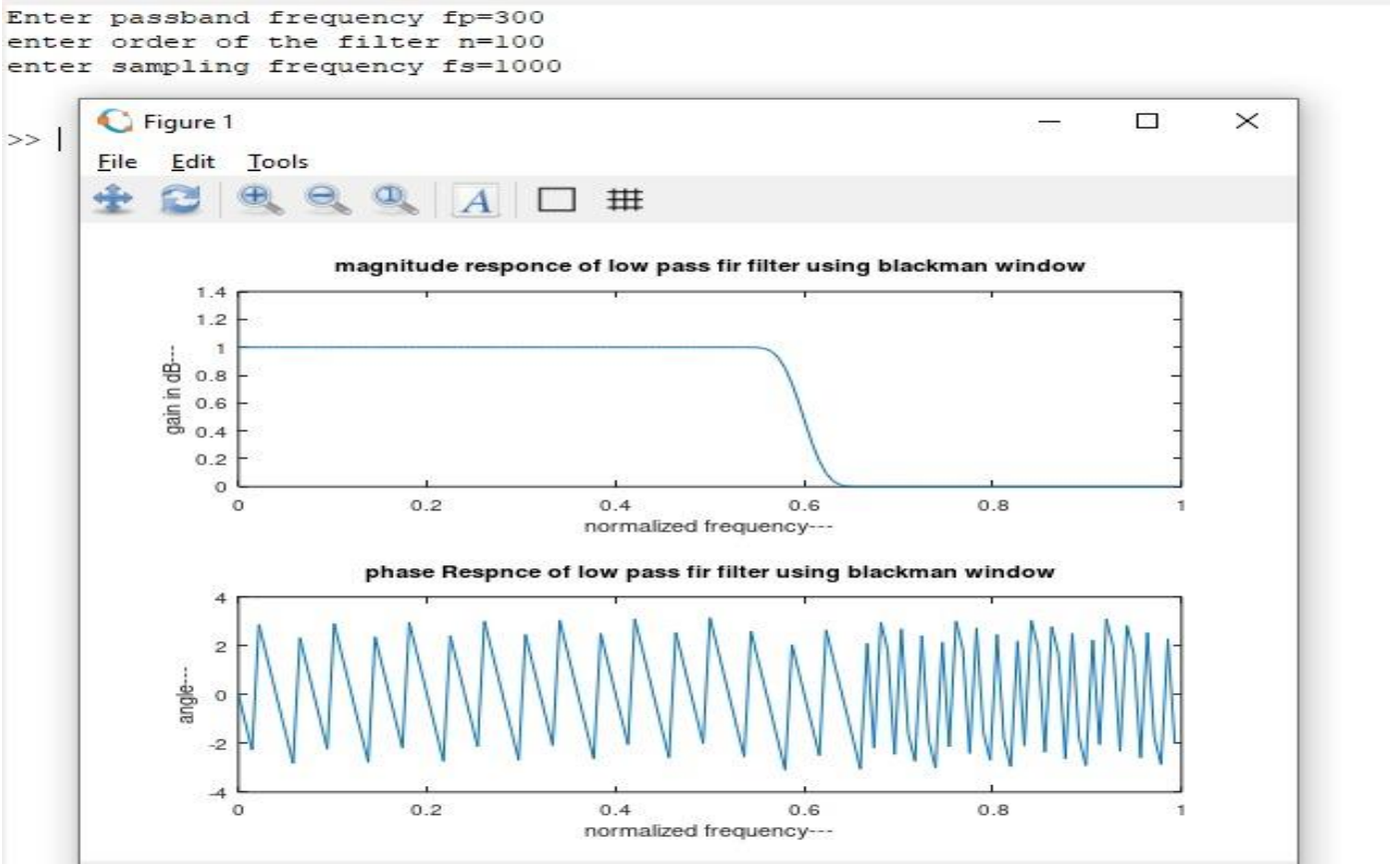

Fig.4: Magnitude and phase response of FIR low pass filter by Windowing function.

3.1 Design FIR HPF by windowing method and plot its magnitude and phase response - MATLAB Program

```
clc;
close all;
clear all;
fp= input ('Enter passband edge normalised freq. wp=');
n= input ('Enter order of filter=');
ps= input ('Enter sampling freq');
fn= 2*fp/ps;
window = blackman(n+1); %boxer, bartlett, hanning,hamming,(use
at place of blackman)
b = fir1(n,fn,'high',window);
[h,w] = freqz(b,1,128);
Subplot(2,1,1);
plot(w/pi,abs(h));
title('Magnitude response of HPF using Blackman window');
Xlabel('Normalised freq…');
Ylabel('gain in dB…');
Subplot(2,1,2);
plot(w/pi,angle(h));
title('phase response of HPF using Blackman window');
Xlabel('Normalised freq…');
Ylabel('angle…');
```

3.2 Simulation Results of FIR Filter

The design of four LPF with different specifications on different accelerators is considered to determine the efficiency optimization technique of power. Two different stop band attenuations, As, of 30 dB and 40 dB are achieved by implementing either 8-bit or 10- bit multipliers.

3.3 FIR Accelerator

There are two greatest topologies in frequency of clock evaluated. These four filters' specification of design, as well as accelerators used. The resulting coefficients were utilized as starting points for applying, which allows for a mistake in relaxed specification. Finally, consumption of compared to the baseline filter's consumption of power and power coefficients is measured. For comparison, the effective dynamic power savings on the full FIR filters and the dynamic power save on the multipliers

To update the pathways connecting registers have constant latency and all registers receive the same clock signal, resulting in perfect synchronization. The presence of dynamic timing margins in a digital circuit is characterized by the presence of variation of time due to slow change of environment. The time of a digital circuit is also characterized by the presence of dynamic margins.

Further timing and power improvements. To leverage dynamic timing margins and for timing monitoring, circuits and techniques are proposed:

• For the exploitation of dynamic timing margins, generate a capable of making instantaneous and free glitch modifications to the period of clock is required.

• It displays monitor the time in which design at runtime is identify setup of timing violations.

Power savings in the filters are slightly less than the projected power savings in the multipliers, because the proposed technique has no effect on the consumption of power in the registers, clock-distribution network, adders, buffers. The proposed power optimization technique's efficacy has also been assessed using both HPF and a BPF design.

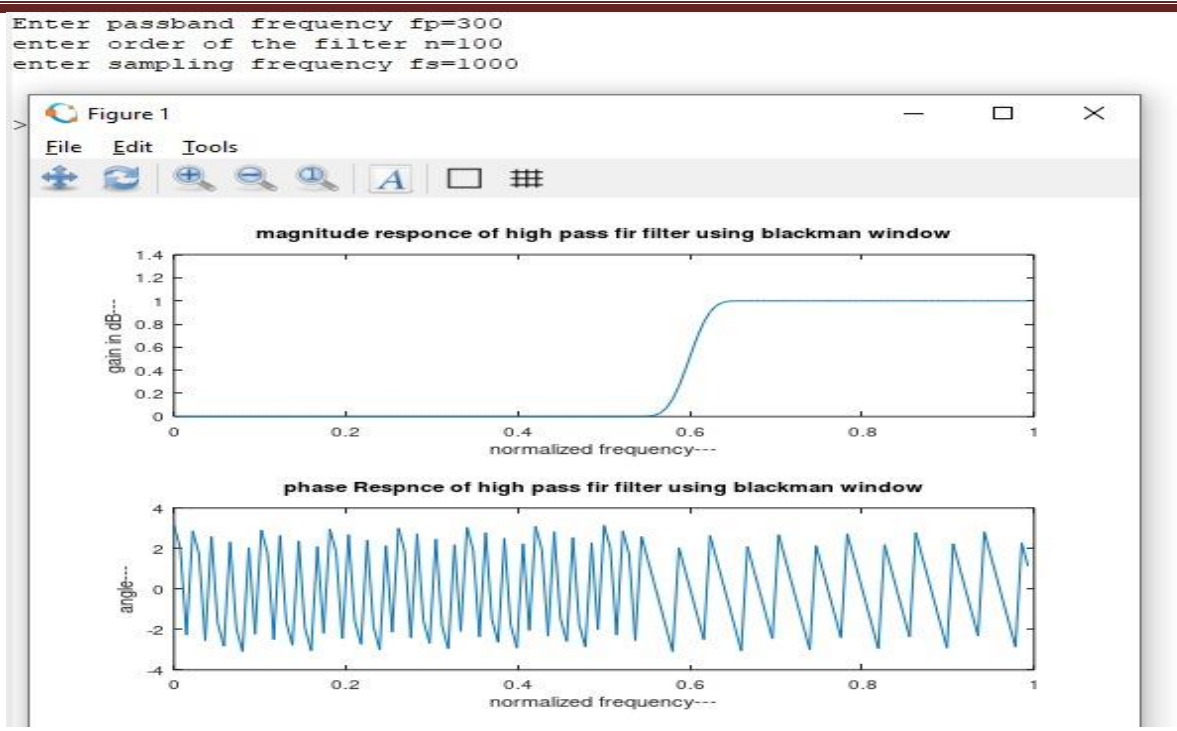

Fig. 5: Magnitude & phase response of FIR High pass filter by Windowing function.

3.4 Power Savings

The potential for power savings is the primary reason for employing DET clocking. An accurate power analysis was performed on each of the three test blocks. The resultant power numbers show the power consumption for both clocking systems. For each case study, the simulated clock frequency in the DET design is half of the SET clock frequency to provide similar throughput in both implementations. The consumption of power are divide into register and combinatorial logic ,as well as a total power usage summary. To lay the groundwork for a more in-depth investigation, each bar in the plot is further divide into internal power, switching power, and leakage power.

4.Conclusions

In this Paper, analysis of sequential circuit (D This part illustrated potential of Failure due to overlapping of clock in which DET-FFs use transmission gates as output MUX, exhibiting without rate of error at Vth is 40 nm in CMOS technology. In this area static TSPC Dual edge triggered flip flop eliminates the overlapping the clock changes, and across temperature. Furthermore, among popular DET-FF registers, the register provide power-delay product and CK-to-Q delay.

References

[1]. YM Lee, G Shin. True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near- Threshold Voltage Operation in IoT Applications, IEEE Access, 2020.

[2]. Bonetti, N Preyss, A Teman, A Burg. Automated Integration of Dual-Edge Clocking for Low- Power Operation in Nanometer Nodes, ACM Transactions on Design Automation of Electronic Systems, 2017.

[3]. Bonetti, A Teman, P Flatresse, A Burg. Multipliers-Driven Perturbation of Coefficients for Low-Power Operation in Reconfigurable FIR Filters, IEEE Transactions on Circuits and Systems Regular Papers, 2017.

[4]. Bonetti, Andrea, A Teman, A Burg. An overlap-contention free true-single-phase clock dual-edge-triggered flip flop, IEEE International Symposium on Circuits and Systems (ISCAS), 2015.

[5]. A Bonetti, Roman Golman, R Giterman, A Teman, A Burg. A Timing-Monitoring Sequential for Forward and Backward Error-Detection in 28 nm FD-SOI, IEEE International Symposium on Circuits and Systems (ISCAS), 2018 Andrea Bonetti, Roman Golman, Robert Giterman, Adam Teman, Andreas Burg. Gain-Cell Embedded DRAMs: Modeling and Design Space, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020 Publication

[6]. R Giterman, A Bonetti, EV Bravo, T Noy, A Teman, Andreas Burg. Current-Based Data- Retention-Time Characterization of Gain-Cell Embedded DRAMs Across the Design and Variations Space, IEEE Transactions on Circuits and Systems I: Regular Papers, 2020.

[7]. K Lundager, B Zeinali, M Tohidi, J Madsen, F Moradi. Low Power Design for Future Wearable and Implantable Devices, Journal of Low Power Electronics and Applications, 2016.